**四川大学期末考试试题（闭卷）**

**（2019——2020学年第 1 学期） B卷**

课程号：304131030 课序号： 课程名称：数字逻辑（双语） 任课教师： 成绩：

适用专业年级：2019级 学生人数： 印题份数： 学号： 姓名：

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| **考 生 承 诺**  我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：  1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；  2、不带手机进入考场；  3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。  **考生签名：** |
| 1. Choose the best answer from the four choices(20 points, 2 points per question).    1. The output of an OR gate is LOW when ( ).   A. any input is HIGH B. all inputs are HIGH C. no inputs are HIGH D. Both (a) and (b)   * 1. The two types of gates which are called universal gates are （）   A. AND/OR B. NAND/NOR C. AND/NAND D. OR/NOR   * 1. According to DeMorgan's theorems, which of the following is correct? ( )   A. B. C. D. all of above   * 1. If the output of a three-input AND gate must be a logic LOW, what must the condition of the inputs be? ( ). A. All inputs must be LOW; B. All inputs must be HIGH;   C. At least one input must be LOW; D. At least one input must be HIGH;   * 1. Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate? ( )   A. B.    C. D.     * 1. Which is a correct 8421BCD code? ( ) A. 00101000 B. 11011001 C. 100 D. 0101100001 |

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| * 1. The 4-2 priority encoder is shown as following and I3’s priority is highest and I0’s priority is lowest, the output Y1Y­ is ( ) when I3I2I1I0 = 0101. A. 00 B. 01 C. 10 D. 11   2. Which of the following combinations of logic gates can decode binary 1101 with active-LOW? ( )   A. One 4-input AND gate B. One 4-input AND gate, one inverter  C. One 4-input AND gate, one OR gate D. One 4-input NAND gate, one inverter   * 1. The code that has an even-parity error is （ ）.   A. 111100 B. 001010 C. 101110. D. 111000   * 1. A modulus-9 ring counter requires ( )   A. 4 flip-flops B. 9 flip-flops C. 12 flip-flops D. 5 flip-flops   1. Fill in the blanks with the correct answer.(20 points, 2 points per blank) 2. Covert the following numbers to the indicated radix numbers   A. (110111.1)2 = (\_\_\_\_)10 B. (01000101.011000100101)BCD = (\_\_\_\_)8   1. The standard SOP form of is\_\_\_ \_\_\_\_\_\_\_.. 2. Simply the Boolean expression . The answer is \_\_\_\_\_ \_\_. 3. If both inputs of a 2-input NOR gate are connected, the gate will function as an \_\_ \_\_\_. 4. The 3-8 Decoder(74LS138) is designed as Figure2(5) and the logical expression of Y represented by the logical variables A, B and C is\_\_\_\_ \_\_\_\_\_\_\_\_\_     Figure 2(5)   1. If the present state is 100, after 3 clock pulses, the state of a 3-bit up/down counter in the DOWN mode is\_\_\_\_ 2. The characteristic equation of SR latch is \_\_\_ \_\_ 3. The maximum counting length (base number) of a counter which consists of N flip-flops is\_\_\_. 4. The reset state of a D latch occurs when \_\_\_\_ \_\_\_. 5. Answer the questions briefly(40 points, 8 points per question).    1. As shown in the circuit:       1. Develop the truth table and write the Boolean expression.(4 points)       2. Implement it with a 4-1 MUX. (4 points)     Figure 3(1)  解答：1）     * 1. Design a 3-input voting system with **NAND gate only**, the system has a active-HIGH output when 2 or more “yes” are voted.      1. Write down the input and output variables and their values (2 points)      2. Develop the truth table(2 points).      3. Write the expressions and draw the logic diagram(4 points).   解答：     * 1. Simplify the following logic functions with a Karnaugh map.      1. f(w, x, y, z)= y’z + w’xy’ + w’xy + xy’z (4 points)      2. (4 points)   解答：   * 1. As shown in Figure 3(4), try to draw the waveforms of output B and C, FF1 and FF2 are initialized with 0.     Figure 3(4)   * 1. A rising-edge clocked serial in/serial out shift register has a data-output waveform as shown in the following figure. What binary number is stored in the 8-bit register after eight clock pulses if the first data bit out (left-most) is the LSB.     Figure 3(5)  解答：   1. Comprehensive questions(20 points, 10 points per question).    1. Design a circuit to detect a one-decimal-number(using 8421BCD code). If the number is less than or equal to 4 output 0, greater than 4 output 1. (open answer)    2. Design a counter to produce the following sequence: 3, 6, 12, 9, 3, …(open answer) |

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